Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-9. (Canceled)

10. (Previously Presented) A phase change memory cell, comprising:

a cup-shaped resistive element having a substantially vertical wall, said vertical wall having a top surface of sublithographic thickness;

a delimiting structure, having an aperture over said resistive element; and

a memory portion of a phase change material, housed in said aperture, said memory portion being in direct electrical contact with the top surface of the vertical wall of the cup-shaped resistive element and defining a contact area of sublithographic extension;

wherein said memory portion is sealed inside said aperture by a sealing structure directly lying on said delimiting structure.

11. (Original) A phase change memory cell according to claim 10, wherein said delimiting structure comprises at least a dielectric layer.

12. (Original) A phase change memory cell according to claim 11, wherein said sealing structure lies directly on said dielectric layer.

13. (Original) A phase change memory cell according to claim 11, wherein said delimiting structure comprises adhesion portions interposed between said dielectric layer and said sealing structure.

14. (Original) A phase change memory cell according to claim 10, wherein said memory portion is aligned with said delimiting structure.

15. (Original) A phase change memory cell according to claim 10, wherein said sealing structure comprises a stack of conducting layers.

16. (Original) A phase change memory cell according to claim 10, wherein said resistive element includes a first thin portion having a first sublithographic dimension in a first direction and said memory portion has a second sublithographic dimension in a second direction transverse to said first direction; said contact area of sublithographic extension having substantially said first sublithographic dimension in said first direction and said second sublithographic dimension in said second direction.

17. (Previously Presented) The memory cell according to claim 16, wherein said memory portion has a substantially elongated shape with a main dimension extending parallel to said first direction.

18. (Canceled)

19. (Original) A phase change memory cell according to claim 10 wherein said aperture is a slit.

20. (Previously Presented) A memory device comprising:

a selection element; and

a phase change memory element coupled to said selection element, said phase change memory element having a cup-shaped resistive element having a substantially vertical wall, said vertical wall having a top surface of sublithographic thickness; a delimiting structure having an aperture over said resistive element; and a memory portion of a phase change material, housed in said aperture, said resistive element and said memory portion being in direct electrical

contact and defining a contact area of a first dimension of less than 100nm and a second dimension of less than 100nm, said second dimension being substantially perpendicular to said first dimension, wherein said memory portion is sealed inside said aperture by a sealing structure directly lying on said delimiting structure.

21. (Original) A memory device according to claim 20 wherein said selection element is a transistor.

22. (Original) A memory device according to claim 20 wherein said selection element is a diode.

23. (Original) A memory device according to claim 20 wherein said aperture is a slit.

24. (Currently Amended) A memory device comprising:

a first cup-shaped resistive element having a substantially vertical wall, said vertical wall having a top surface of sublithographic thickness;

a second cup-shaped resistive element having a substantially vertical wall, said vertical wall having a top surface of sublithographic thickness;

a delimiting structure with an aperture having a first portion over the first resistive element and a second portion over the second resistive element;

a first memory portion of phase change material in the first portion of said aperture, the first memory portion being in contact with the first resistive element and defining a first contact area of sublithographic dimension~~,~~; ~~and~~

a second memory portion of phase change material in the second portion of said aperture, the second memory portion being in contact with the second resistive element and defining a second contact area of sublithographic dimension; and

a sealing structure directly lying on said limiting structure, sealing the first memory portion and the second memory portion in said aperture.

25. (Canceled)

26. (Original) The memory device according to claim 24 wherein said aperture is a slit.

27. (Previously Presented) The memory device according to claim 10 wherein a width of contact area is substantially the same as the thickness of the vertical wall of the cup-shaped resistive element.

28. (Previously Presented) The memory device of claim 10 wherein the cup-shaped resistive element is filled, within the substantially vertical wall, with a dielectric material.

29. (Previously Presented) A memory device comprising:

a resistive element having a top surface, an elongated-shaped portion of said top surface having a first width of sublithographic dimension;

a delimiting structure overlying and transversing the elongated-shaped portion of the top surface of the resistive element, the delimiting structure defining a slit having a second width of sublithographic dimension,

a phase change material in the slit and in direct electrical contact with the resistive element by a contact area, said contact area having a first dimension substantially the same as the first width of the resistive element, and a second dimension substantially the same as the second width of the slit; and

a sealing structure directly lying on said delimiting structure sealing the phase change material within the slit.

30. (Previously Presented) The memory device of claim 29 wherein the first dimension of the contact area is about 60nm or less, and the second dimension of the contact area is about 60nm or less.

31. (Previously Presented) The memory device of claim 29 further comprising a selection element.